

What is claimed is:

1. A serial data receiver comprising:

a differential receiver configured to receive first and second

5 signals of opposite phases to provide a differential signal

of the first and second signals as received serial data;

a clock generator configured to generate a clock signal;

a tracking circuit configured to receive the received serial

data and the clock signal to generate a synchronous clock

10 signal based on the clock signal by tracking the received

serial data, the tracking circuit configured to generate

a synchronous serial data synchronized with the

synchronous clock signal;

an idle detector configured to receive the first signal and

15 the second signal, the idle detector configured to detect

an idle period of the first and second signals to provide

an idle signal;

a memory configured to store the serial data in response to

transitions in the synchronous clock signal, the memory

20 configured to provide the stored data in response to

transitions in the clock signal, the memory configured to

stop storing based on a hold signal; and

a data protector configured to receive the idle signal to

generate the hold signal, the data protector configured

25 to provide the hold signal for the memory.

2. The serial data receiver of claim 1, wherein:  
the idle detector provides the idle signal when the first and  
second signals become in-phase.

5 3. The serial data receiver of claim 1, wherein:  
The memory stores the serial data into a register in the memory.

4. The serial data receiver of claim 1, wherein:  
the clock generator is a phase-locked loop oscillator.

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5. The serial data receiver of claim 1, wherein:  
the data protector provides a hold signal that puts the memory  
in an input prohibited state from the detection of an end  
of the serial data to the stoppage of the idle signal.

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6. The serial data receiver of claim 1, wherein the data  
protector comprises:

a data end detector configured to receive the synchronous  
serial data to detect an end of the synchronous serial data,  
the data end detector configured to provide a data end  
signal based on the end of the synchronous serial data;  
and

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a hold controller configured to receive the idle signal and  
the data end signal to generate hold signal, the hold  
controller configured to provide the hold signal to stop  
storing of the memory from a timing that detection of data

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end based on the data end signal to a timing that detection of next data based on the idle signal.

7. A serial data receiver comprising:

- 5 a differential receiver configured to receive first and second signals of opposite phases to provide a differential signal of the first and second signals as received serial data;
- a clock generator configured to generate a clock signal;
- a tracking circuit configured to receive the received serial  
10 data and the clock signal to generate a synchronous clock signal based on the clock signal by tracking the received serial data, the tracking circuit configured to generate a synchronous serial data synchronized with the synchronous clock signal;
- 15 an idle detector configured to receive the first signal and the second signal, the idle detector configured to detect an idle period of the first and second signals to provide an idle signal;
- a memory configured to receive the synchronous clock signal  
20 to store the serial data in response to transitions in the synchronous clock signal, the memory configured to provide the stored data in response to transitions in the clock signal; and
- a data protector configured to receive the synchronous clock  
25 signal and the idle signal to provide the memory with the synchronous clock signal, the data protector configured

to stop providing the memory with the synchronous clock signal based on the idle signal.

8. The serial data receiver of claim 7, wherein:

5 the idle detector provides the idle signal when the first and second signals become in-phase.

9. The serial data receiver of claim 7, wherein:

The memory stores the serial data into a register in the memory.

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10. The serial data receiver of claim 7, wherein:

the clock generator is a phase-locked loop oscillator.

11. The serial data receiver of claim 7, wherein:

15 the data protector stops providing the memory with the synchronous clock signal from detecting the end of synchronous serial data to the end of the idle period.

12. The serial data receiver of claim 7, wherein the data protector comprises:

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a data end detector configured to receive the synchronous serial data to detect an end of the synchronous serial data, the data end detector configured to provide a data end signal based on the end of the synchronous serial data;

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and

a clock controller configured to receive the idle signal and

the data end signal to generate the suspended clock signal ,  
the clock controller configured to provide the suspended  
clock signal to stop operation of the memory from a timing  
that detection of data end based on the data end signal  
5 to a timing that detection of next data based on the idle  
signal.